

## Product Brief

### Intel® 3100 Chipset

Embedded Computing



# Intel® 3100 Chipset

for Dual-Core Intel® Xeon® Processors LV and ULV and Intel® Celeron® Processors 1.66 GHz and 1.83 GHz

## Product Overview

The Intel® 3100 chipset combines server-class memory and I/O controller functions into a single component, creating the first integrated Intel® chipset specifically optimized for embedded, communications, and storage applications. This single-chip system controller replaces a separate memory controller hub and I/O controller hub, significantly conserving board real estate and power consumption.

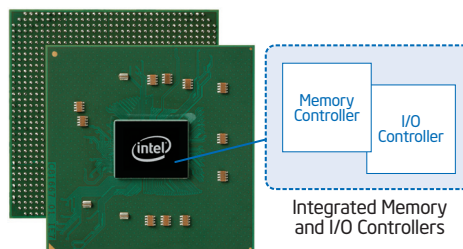
The 667 MHz front-side bus (FSB) supports Dual-Core Intel® Xeon® processors LV and ULV and the Intel® Celeron® processors 1.66 GHz and 1.83 GHz addressing the needs of high-performance, low-power platforms within small form factor designs such as PrAMC, Compact PCI\* and COM Express.\* The Dual-Core Intel Xeon processor LV has a thermal design power (TDP) of 31 W; the ULV version has a TDP of 15 W; and the Intel Celeron processor has a TDP of 27 W.

Dual-Core Intel Xeon processors LV and ULV combine the benefits of dual-core processing capability and intelligent power management for improved performance/watt, while the Intel Celeron processors provide value in a single-core solution. These processors support FSB parity and Intel® Virtualization Technology,<sup>1</sup> making them ideal for a wide range of high-performance applications with restricted power requirements.

Along with a strong ecosystem of hardware and software vendors, including members of the Intel® Communications Alliance ([intel.com/go/ica](http://intel.com/go/ica)), Intel helps cost-effectively meet development challenges and speed time-to-market.

## PCI Express

For demanding I/O and networking applications, PCI Express interfaces attach a variety of Intel and third-party I/O solution components and adapters directly to the Intel 3100 chipset (one x8 PCI Express interface and one x4 PCI Express interface). Each interface may be bifurcated to provide additional configuration flexibility. The interfaces provide throughput speeds of up to 4 GB/s on the x8 interface, and up to 2 GB/s on the x4 interface, allowing I/O to keep pace with the rest of the platform.



## Memory

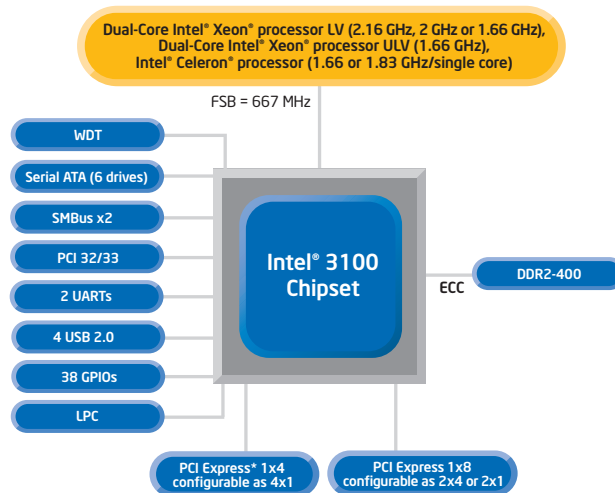
Intel 3100 chipset-based platforms are ECC-enabled and support single-channel DDR2-400 memory (up to 16 GB), which is ideal for storage and memory-intensive applications. The memory subsystem interface supports up to four ranks for a total system bandwidth of 3.2 GB/s.

## Data Protection

The Intel 3100 chipset is designed to bring enterprise-level reliability, availability, serviceability, usability and manageability (RASUM) to the embedded platform. The chipset supports FSB parity and two bits of parity on 64 bits of data on internal buses. The PCI Express interface supports 32-bit cyclic redundancy check (CRC) for detection and automatic recovery of transient signaling errors. Memory interface supports Single Error Correct/Double Error Detect (SEC/DED) ECC, auto retry on uncorrectable errors, and integrates a hardware memory scrubber to scan the populated memory space, proactively seeking out soft errors in the memory subsystem.

## Enhanced Direct Memory Access (EDMA)

A four-channel EDMA controller efficiently moves data within local system memory or from the local system memory to the I/O subsystem. Each EDMA channel provides low-latency, high-throughput data transfer capability with no CPU intervention for higher overall system performance. These transfers may be individually designated to be coherent (snooped on the FSB) or non-coherent (not snooped on the FSB), providing improvements in system performance and utilization when cache coherence is managed by software rather than hardware. EDMA also enables Quality of Service (QoS) by prioritization of data.



## Features

Supports Dual-Core Intel® Xeon® processors LV and ULV

Supports Intel® Celeron® processors (1.66 and 1.83 GHz)

40 mm x 40 mm FC-BGA package

PCI Express\*

DDR2-400 memory interface

Advanced Platform RAS

GPIO

USB 2.0

Two integrated UARTs (Serial Ports)

32/33-bit PCI Bus Interface

SMBus x2

Integrated Serial ATA Host Controllers

Watchdog Timer

Power Management

## Benefits

- Two high-performance cores per platform meet the needs of high-performance, low-power applications with small form-factor constraints

- Single-core solution offers scalable performance and value

- Requires 50% less board space than prior-generation two-chip chipsets<sup>2</sup>

- Direct connection between the Intel® 3100 chipset and PCI Express component/adapters; bandwidth up to 4 GB/s on the x8 PCI Express interface; higher bandwidth and less I/O bottlenecks than PCI-X\*

- Maximum memory bandwidth of 3.2 GB/s

- Decreased power consumption – especially important on dense rack, hot-plug controller and blade configurations

- Memory ECC, SEC/DED, and DIMM scrubbing can improve system reliability

- 32-bit ECRC on PCI Express

- Hot swap PCI Express enhances serviceability

- SMBus port hooks for remote management operation and support for a variety of third-party base management controller and BIOS solutions

- 38 pins (25 dedicated, 13 mux'ed)

- One USB 2.0 host controller with a total of four ports

- Supports wakeup from sleeping in S3 and S5 states

- Supports full function of a standard 16550 UART including hardware flow control interface

- Supports PCI Rev 2.3 specification at 33 MHz

- Supports two request/grant pairs

- First SMBus dedicated as slave; second configurable as master or slave

- Six ports provide independent DMA operation in AHCI mode, four ports support in SATA 1.0a mode

- Multiple modes (WDT and free-running)

- ACPI 2.0 support

Product	Product Code	Thermal Design Power	Package
Intel® 3100 Chipset	LE3100MICH	10.4 – 12.4W	1284 Flip Chip-Ball Grid Array (FC-BGA3)

\*Intel® Virtualization Technology requires a computer system with an enabled Intel® processor, BIOS, virtual machine monitor (VMM) and, for some uses, certain platform software enabled for it. Functionality, performance or other benefits will vary depending on hardware and software configurations and may require a BIOS update. Software applications may not be compatible with all operating systems. Please check with your application vendor.

<sup>2</sup>Comparison with Intel® E7520 Memory Controller Hub plus Intel® 6300ESB I/O Controller Hub

INFORMATION IN THIS DOCUMENT IS PROVIDED IN CONNECTION WITH INTEL® PRODUCTS. EXCEPT AS PROVIDED IN INTEL'S TERMS AND CONDITIONS OF SALE FOR SUCH PRODUCTS, INTEL ASSUMES NO LIABILITY WHATSOEVER, AND INTEL DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY RELATING TO SALE AND/OR USE OF INTEL PRODUCTS, INCLUDING LIABILITY OR WARRANTIES RELATING TO FITNESS FOR A PARTICULAR PURPOSE, MERCHANTABILITY, OR INFRINGEMENT OF ANY PATENT, COPYRIGHT, OR OTHER INTELLECTUAL PROPERTY RIGHT. INTEL MAY MAKE CHANGES TO SPECIFICATIONS, PRODUCT DESCRIPTIONS, AND PLANS AT ANY TIME, WITHOUT NOTICE.

Intel Corporation may have patents or pending patent applications, trademarks, copyrights, or other intellectual property rights that relate to the presented subject matter. The furnishing of documents and other materials and information does not provide any license, express or implied, by estoppel or otherwise, to any such patents, trademarks, copyrights, or other intellectual property rights. Intel products are not intended for use in medical, life saving, life sustaining, critical control or safety systems, or in nuclear facility applications. The Intel® 3100 Chipset may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are available upon request.

Intel, the Intel logo, Intel. Leap ahead. logo, Xeon, and Celeron are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

\*Other names and brands may be claimed as the property of others.

Copyright © 2006 Intel Corporation. All rights reserved.

Printed in USA

1206/KSC/OCG/XX/PDF

♻ Please Recycle

315785-004US

